REMARKS

Applicants appreciate the thorough examination provided in the Office Action mailed September 16, 2005 (hereinafter "Office Action") and the indication that Claims 10 and 11 recite patentable subject matter. In response to this indication of allowability, Applicants have amended Claim 10 to independent form incorporating the recitations of Claims 1 and 9, thus placing Claims 10 and 11 in condition for allowance.

Applicants have also amended independent Claim 1 to overcome the rejections based on Japanese Patent No. 04-093080 to Isao (hereinafter "Isao") and U.S. Patent No. 6,642,130 to Park et al. (hereinafter "Park"). In concert with these amendments, Applicants have canceled Claims 2, 3, 12 and 14, have amended Claims 3-5 and 13 to change their dependencies. Applicants have also amended Claim 9 to correct a typographical error, and have added new Claims 40-50. Applicants submit that the claims, as amended, are patentable over the cited references for at least the reasons discussed below.

Amended Independent Claim 1 is patentable

Claim 1 stands rejected as anticipated by each of Isao and by Park. Applicants have amended Claim 1 to recite:

> A semiconductor device comprising:
> a semiconductor substrate having a recess therein;
> a gate electrode comprising a first portion in the recess and a second reduced-width portion extending from the first portion;
> a source/drain region in the substrate adjacent the recess; and
> a gate insulator interposed between the first portion of the gate electrode and a surface of the recess, the gate insulator comprising a first portion disposed on a sidewall of the recess, in contact with the source/drain region and having a first thickness and a second portion disposed on a bottom of the recess, ***spaced apart from the source/drain region*** and having a second thickness less than the first thickness.

Applicants submit that such recitations are supported by the specification as filed, for example, by the description of FIGs. 8 and 9.

The Office Action cites FIGs. 1(a)-(e) of Isao as teaching "a gate electrode comprising a first portion in the recess and a second reduced-width portion extending from the first portion." Office Action, p. 2. Applicants note, however, that none of the figures from Isao

appear to include first and second gate insulator portions of different thicknesses as recited in amended Claim 1. For at least these reasons, Applicants submit that Claim 1 is patentable over Isao.

Applicants further submit that amended Claim 1 is also patentable over Park. In particular, the Office Action cites FIG. 8 of Park as showing a gate insulator with first and second portions of different thicknesses. Office Action, p. 3. However, FIG. 8 of Park clearly shows that the thinner gate insulator portion 20 contacts the lightly-doped drain region 15. Thus, Park does not disclose or suggest "a second portion disposed on a bottom of the recess ***spaced apart from the source/drain region*** and having a second thickness less than the first thickness." For at least these reasons, Applicants submit that amended Claim 1 is patentable over Park.

New Independent Claim 40 is patentable

New independent Claim 40 recites:

> A semiconductor device comprising:
> a semiconductor substrate having a recess therein;
> a gate electrode comprising a first portion in the recess and a second reduced-width portion extending from the first portion;
> a source/drain region disposed in the substrate and spaced apart from the recess; and
> a substantially uniform gate insulator layer lining the recess and interposed between the first portion of the gate electrode and a portion of the substrate between the recess and the source/drain region.

Applicants submit that new Claim 40 is supported by the disclosure of the application as filed, for example, by the description of FIG. 10.

The cited references fail to disclose or suggest the recitations of Claim 40. For example, neither Isao nor Park disclose or suggest "a source/drain region disposed in the substrate and ***spaced apart from the recess***," as each of these references show source/drain regions that immediately adjoin the recesses shown therein. Neither Isao nor Park disclose or suggest "a substantially uniform gate insulator layer lining the recess and ***interposed between the first portion of the gate electrode and a portion of the substrate between the recess and the source/drain region***."

The dependent claims are patentable

Applicants submit that dependent Claims 3-9, 13, 15-17 and 41-50 are patentable at least by virtue of the patentability of the various ones of independent Claims 1 and 40 from which they depend. Applicants further submit that several of these dependent claims are separately patentable.

Claim 4, which stands rejected as obvious over a combination of Isao and U.S. Patent No. 6,255,202 to Lyons et al. (herein after "Lyons") recites "a nitride liner disposed between the first portion of the gate insulator and the recessed portion of the gate electrode." The Office Action concedes that Isao does disclose such recitations, but cites columns 4 and 6 of Lyons as providing the missing teachings. Office Action, p. 4. Applicants note that the cited last paragraph of column 4 refers to FIG. 2 of Lyons merely shows an oxide layer 64 on a silicon layer 62, and shows no gate electrode or gate insulator. The cited first paragraph of column 6 refers to FIG. 8 of Lyons, which shows a polysilicon layer 66 and an insulating layer 68 on the oxide layer 64. There simply is no disclosure or suggestion of the recited nitride liner in this material. In addition, the nitride spacers 74 referred to in the Office Action are temporary features that are removed in a subsequent process, and are not part of the final device structure. *See* Lyons, column 6, lines 32-33. Thus, Lyons does not provide the teachings alleged and, for at least these additional reasons, Applicants submit that Claim 4 is patentable. Similar arguments support the separate patentability of Claim 6.

Conclusion

Applicants respectfully submit that the claims are now in condition for allowance for at least the reasons presented above. Applicants, therefore, request allowance of the claims and passing of the application to issue in due course. Applicants encourage the Examiner to resolve any outstanding issues by contacting the undersigned by telephone.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on January 11, 2006.

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